

High Sensitivity CMOS Limiting Transimpedance Amplifier for 10+ Gbps Applications

Main Features

- Typical -20.3 dBm SM AOP sensitivity at 10.3 Gbps ($C_{PD} = 110$ fF, ER 10 dB, BER 10^{-12})
- Typical -15.3 dBm MM OMA sensitivity at 10.3 Gbps ($C_{PD} = 250$ fF, ER 3 dB, BER 10^{-12})
- Compatible with multi-mode & single-mode PIN photodiodes
- 4.8kΩ differential transimpedance
- No PINK decoupling capacitor required
- +3.3V supply. Typical 30 mA supply current
- Compact 900um x 711um die

Applications

- 10GbE SR/LR/ER Transceivers
- 8xFC/10xFC Transceivers
- OC-192 SONET Receivers
- CPRI/OBSAI 6G/10G Wireless Basestation
- CPRI (Rate 9) 12.165Gbps standard

Product Overview

The HLR10G0 is a 'State of the Art' high sensitivity limiting transimpedance amplifier manufactured in an advanced CMOS process.

With 4.8kΩ transimpedance and differential CML outputs with 50 ohm back termination the HLR10G0 is designed to interface with a wide range of limiting amplifiers. It typically consumes only 30 mA supply current from a single 3.3V power supply.

The HLR10G0 includes a Receiver Signal Strength Indicator (RSSI) monitor function (supporting SFF-8431/8472) that is configurable for sink or source output.

The HLR10G0 features a compact die size, which together with on-chip supply filtering, no PINK decoupling requirement, and reduced bond count enables simple, low cost, high volume optical receiver assemblies.

HiLight has successfully tested the HLR10G0 TIA at 12.165 Gbps for use in CPRI 12G applications.

Block Diagram

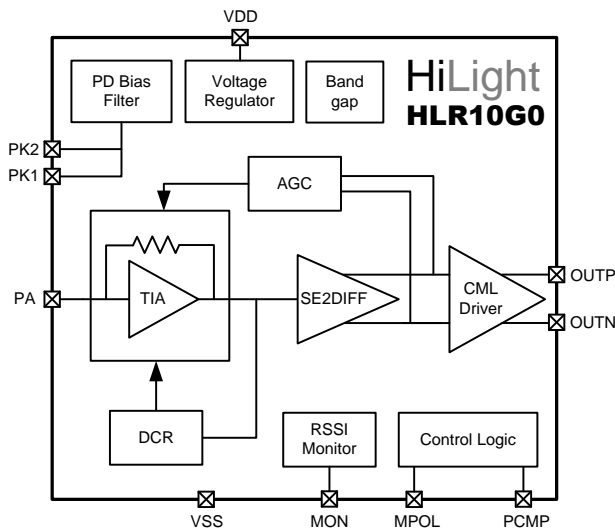


Figure 1 – HLR10G0 Block diagram

Pad Out

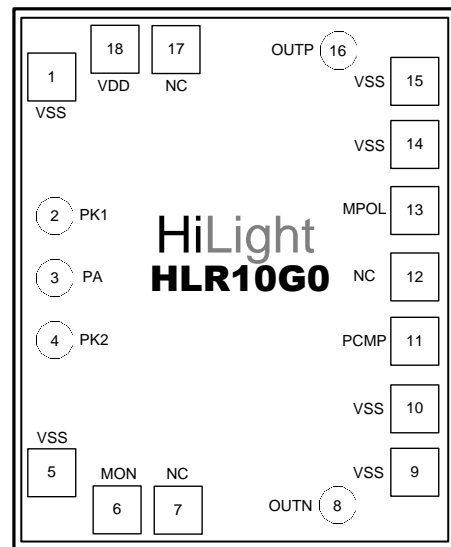


Figure 2 – HLR10G0 Pad Out

Ordering Information

Part Number	Package
HLR10G0-WP	400 known good die in waffle tray packs
HLR10G0-WP-2K	2,000 known good die in 5 stacked waffle tray packs (5 x 400)
HLR10G0-GRP6-5K	4" reconstructed wafer of 5,000 known good die on an 8" grip ring
HLR10G0-GRP6-10K	6" reconstructed wafer of 10,000 known good die on an 8" grip ring

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